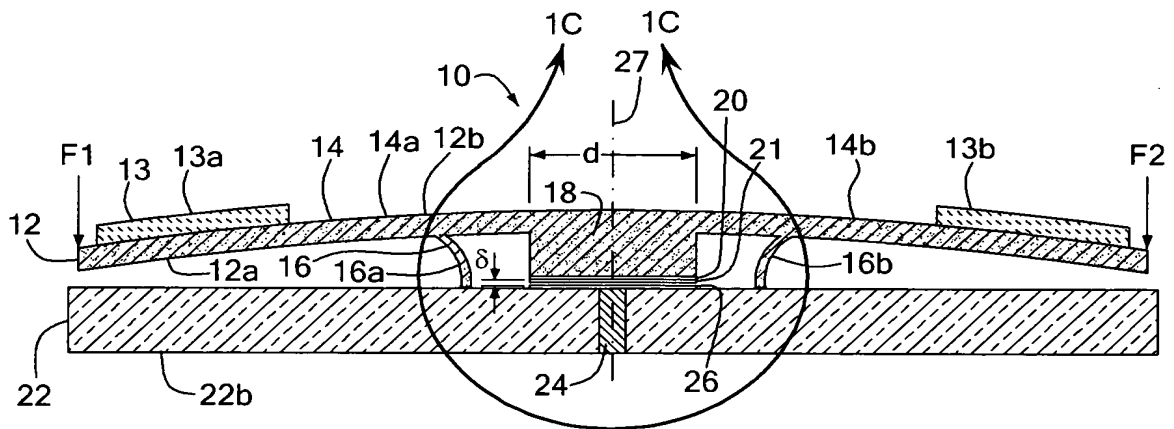
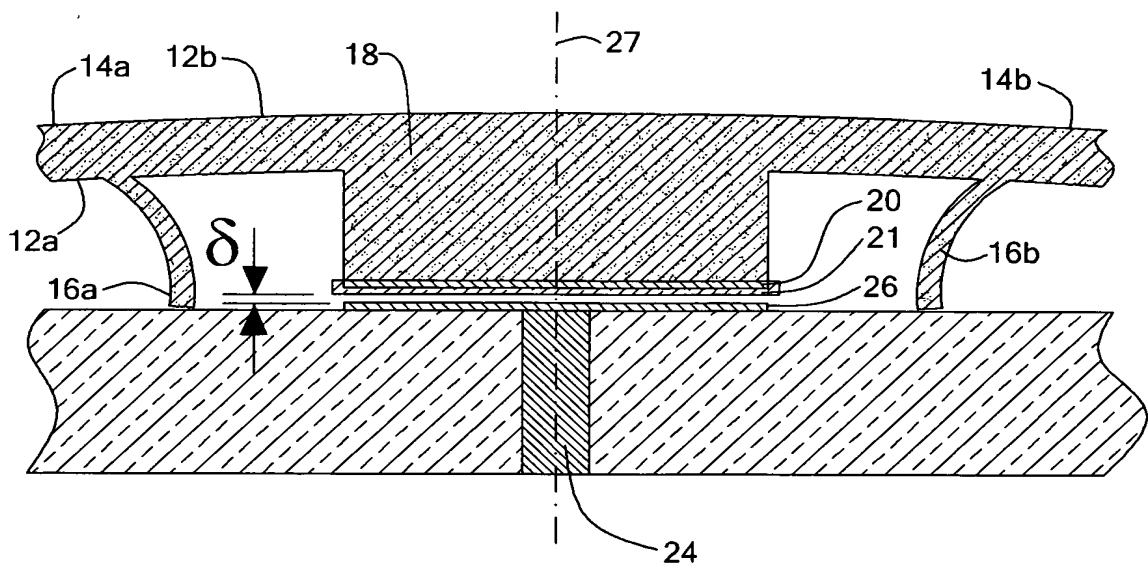


**FIG. 1A**



**FIG. 1B**



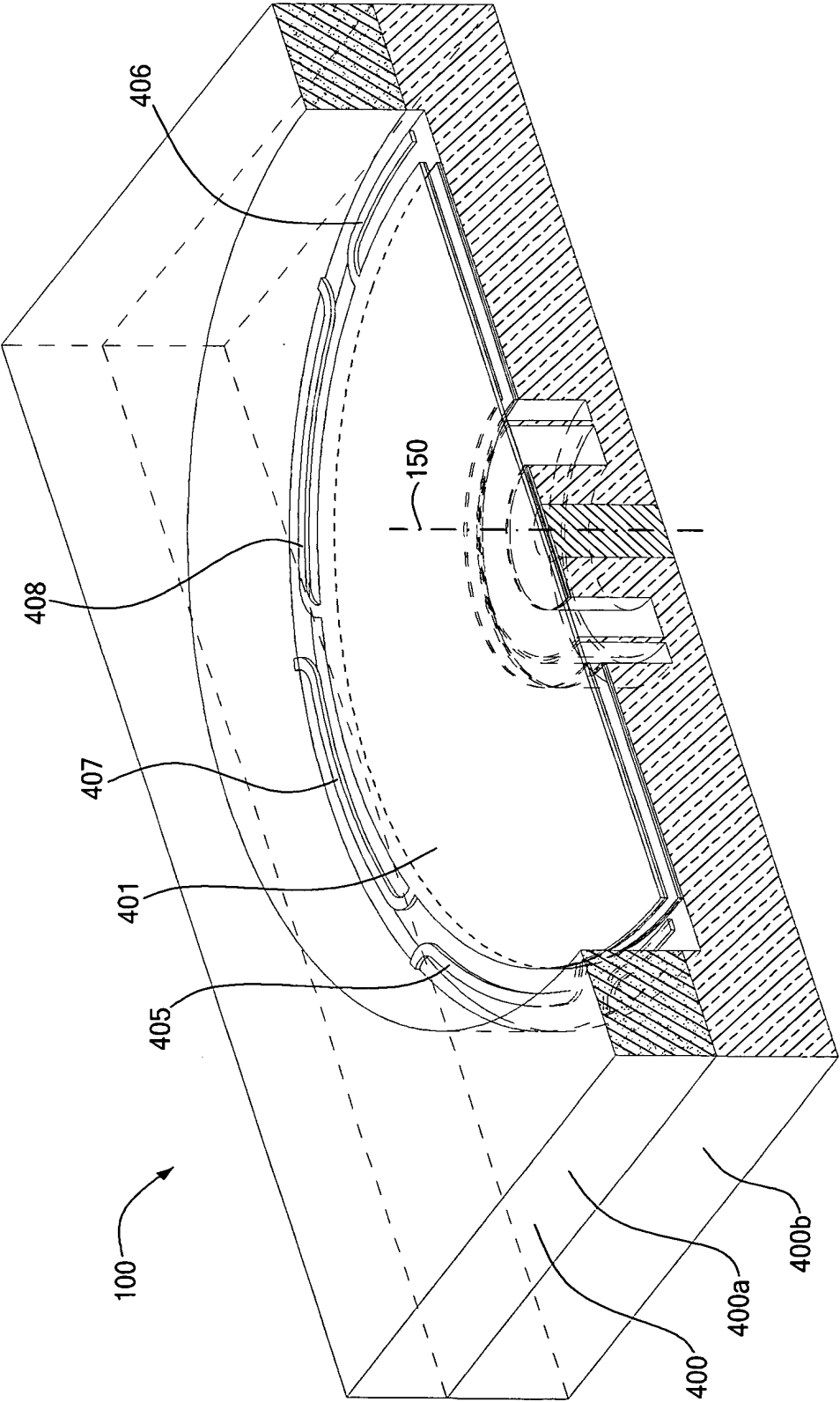
**FIG. 1C**

**FIG. 2A**

**FIG. 3**

**FIG. 4**

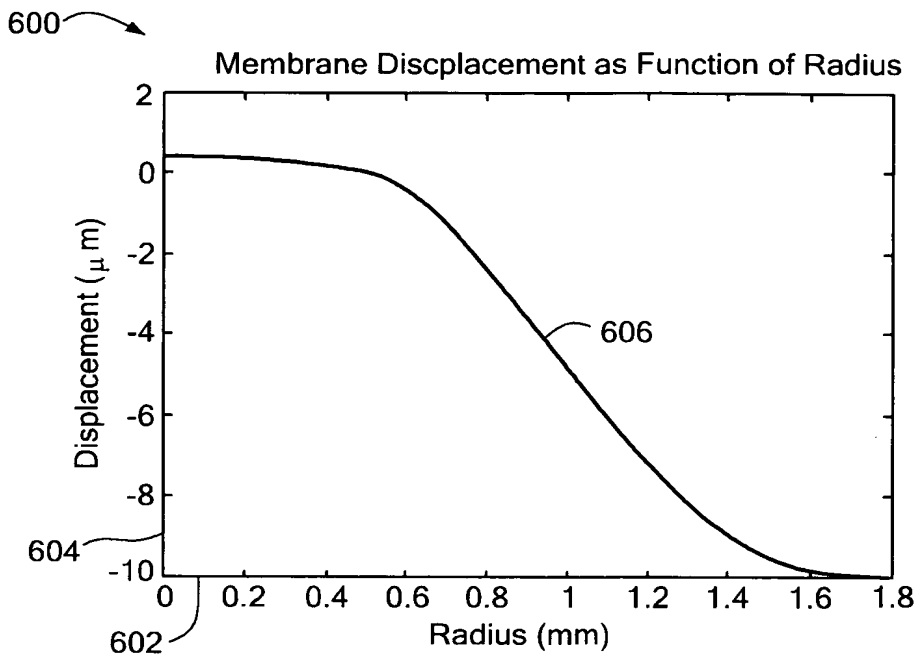
**FIG. 4A**



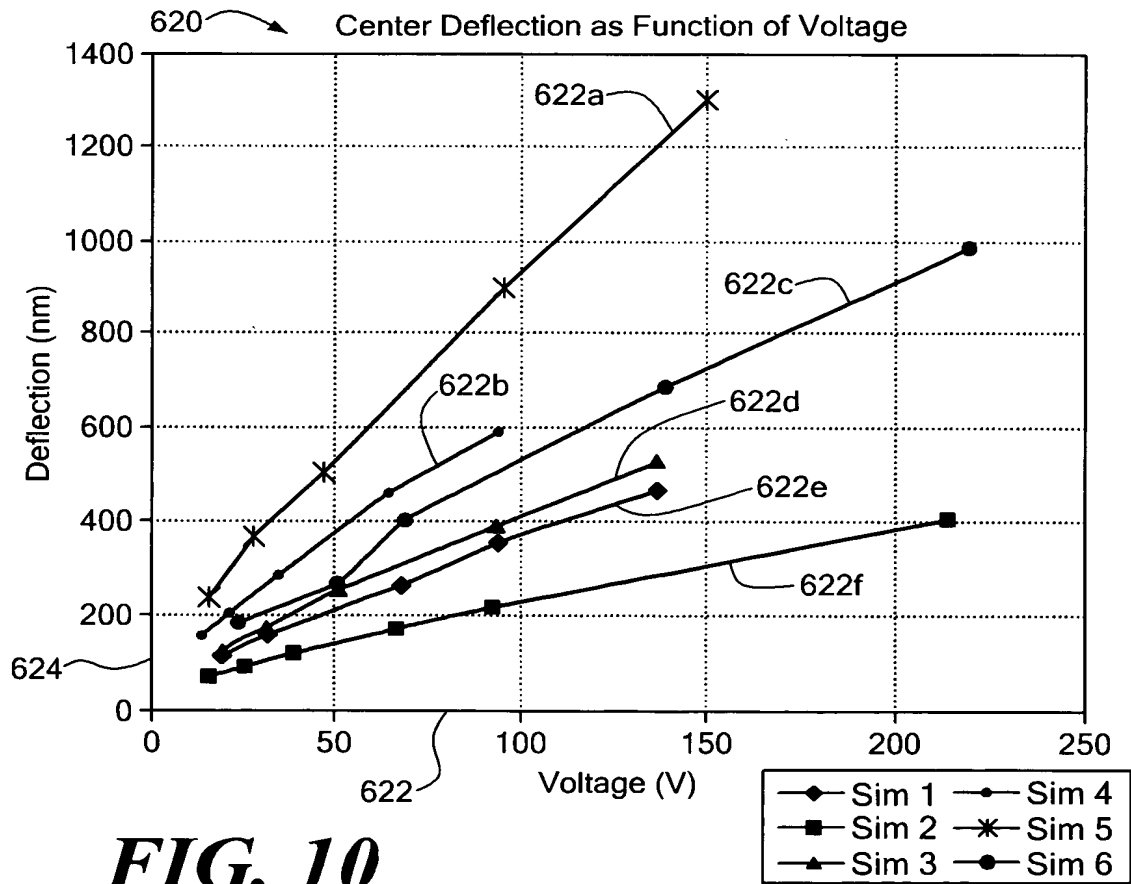
**FIG. 5**

**FIG. 8**

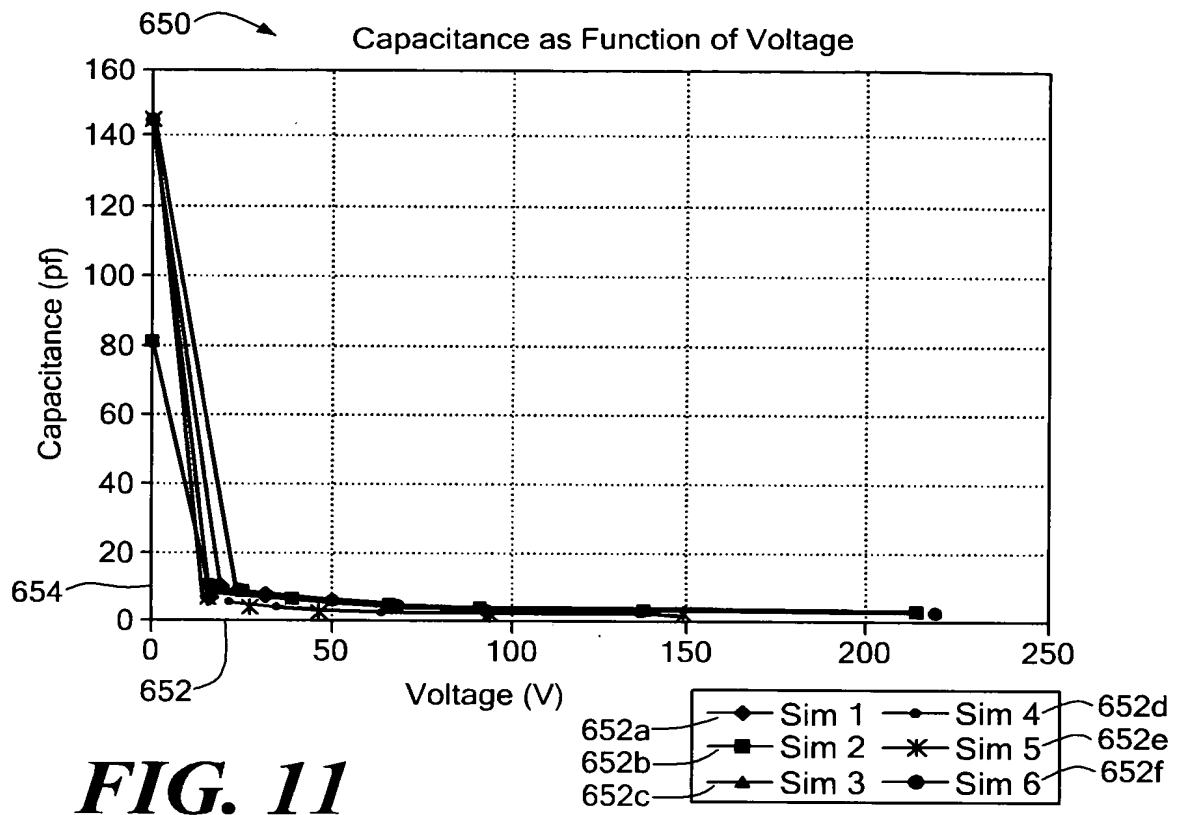




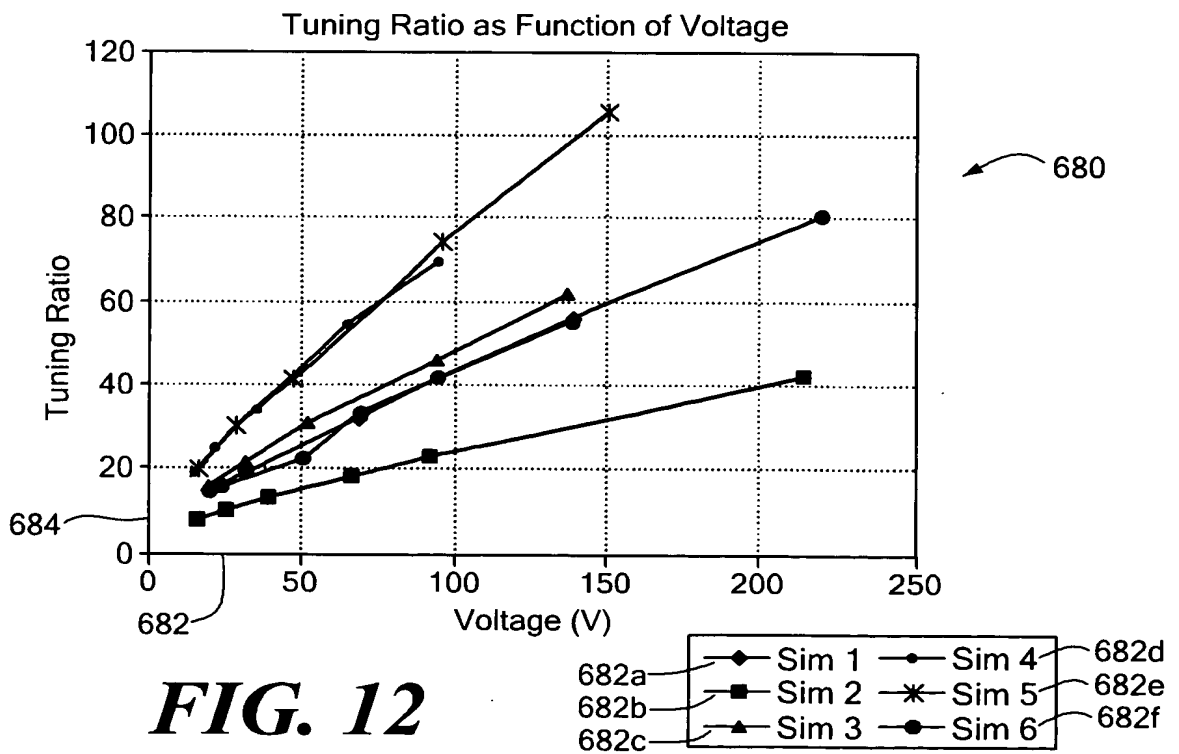
**FIG. 9**



**FIG. 10**



**FIG. 11**



**FIG. 12**

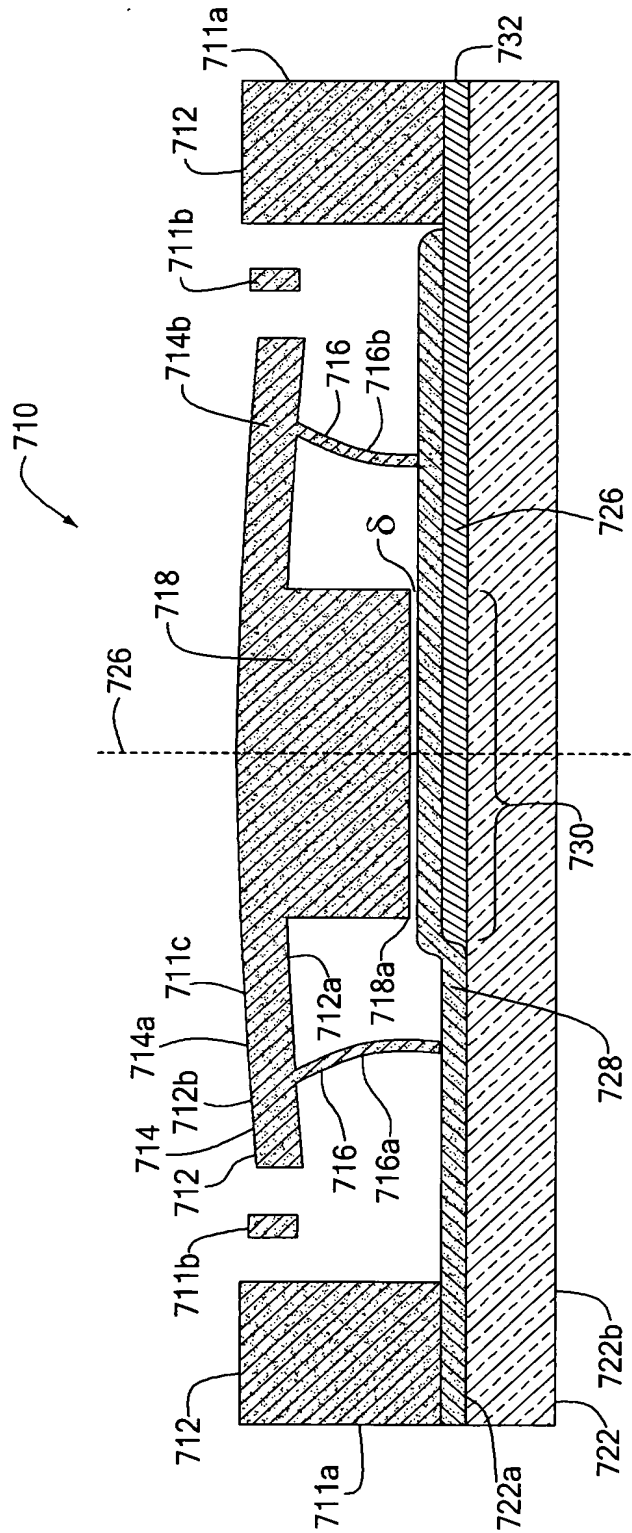
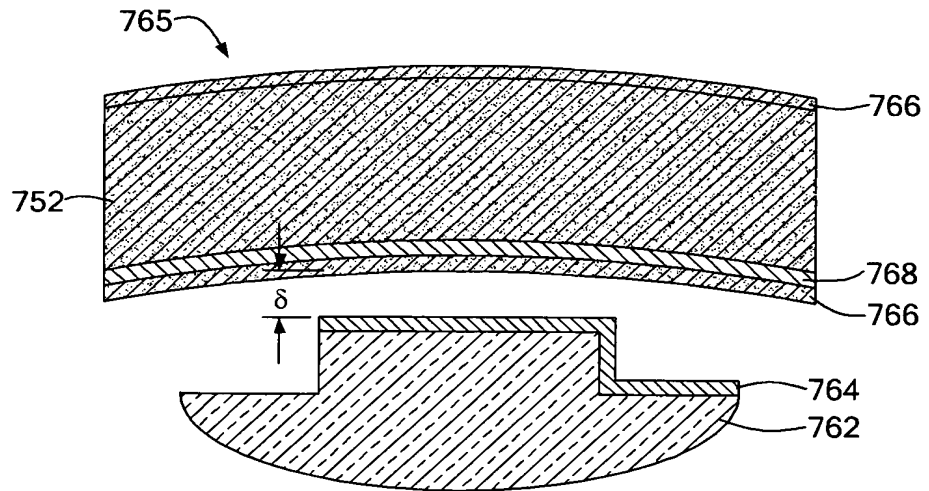
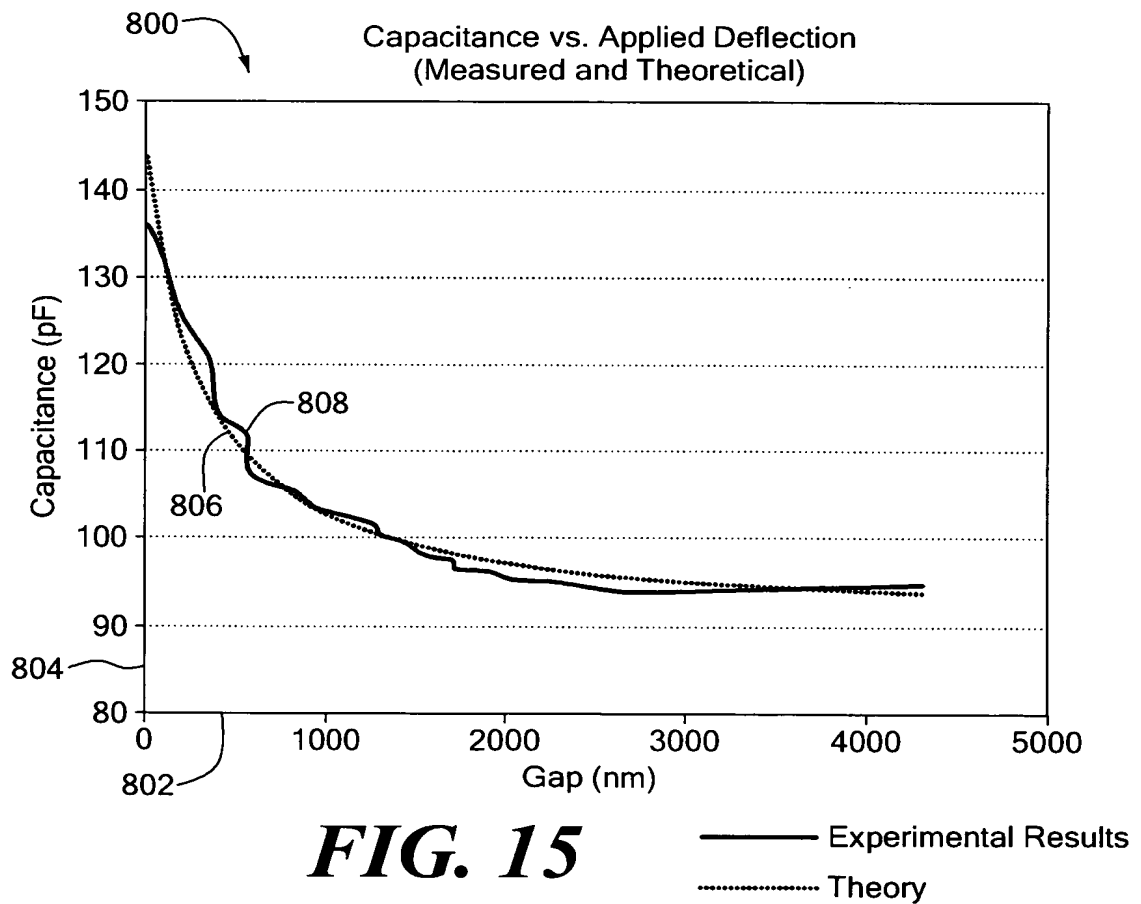


FIG. 14A

**FIG. 14**



**FIG. 14A**



**FIG. 15**

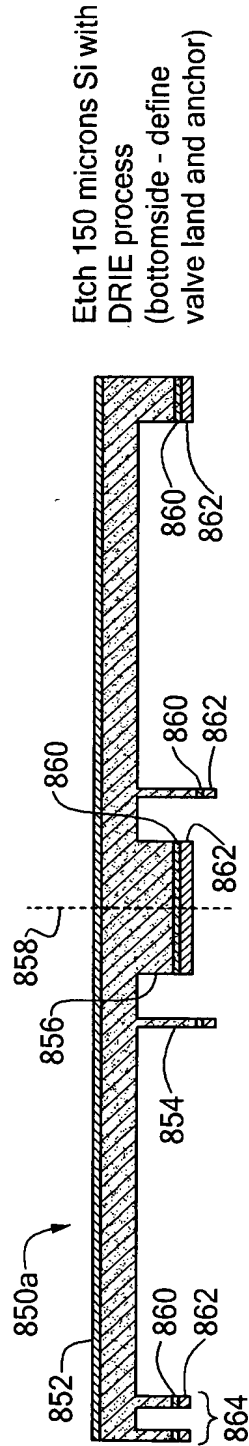


FIG. 16

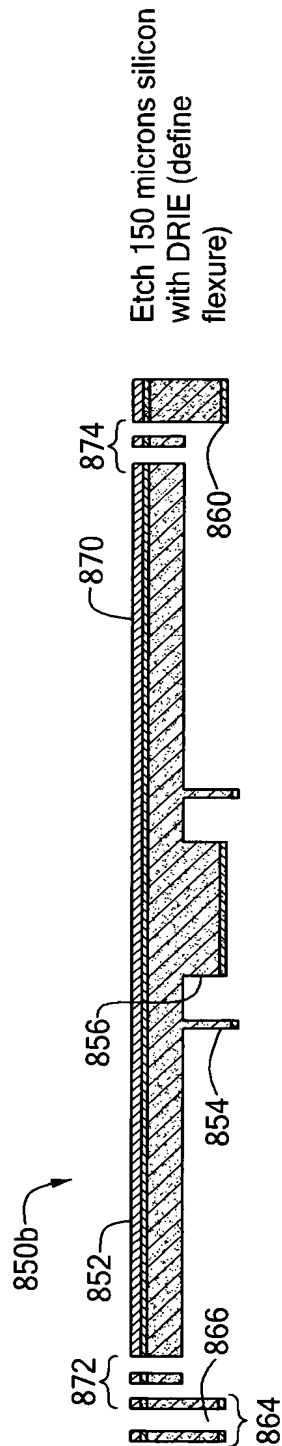


FIG. 16A

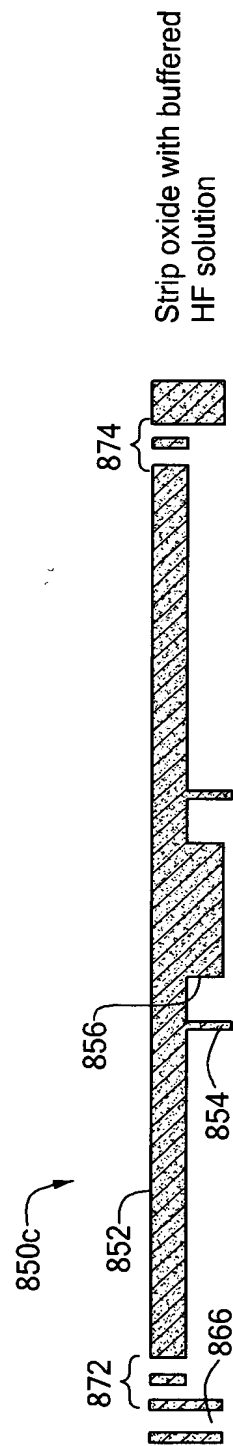


FIG. 16B

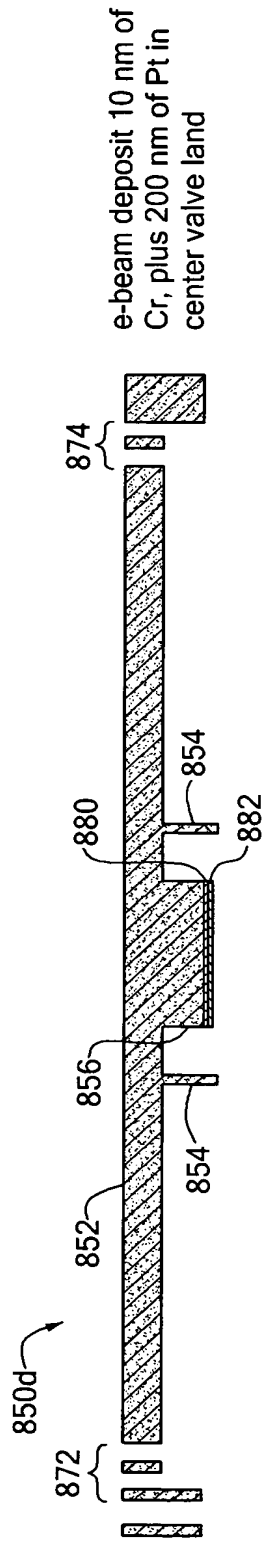


FIG. 16C

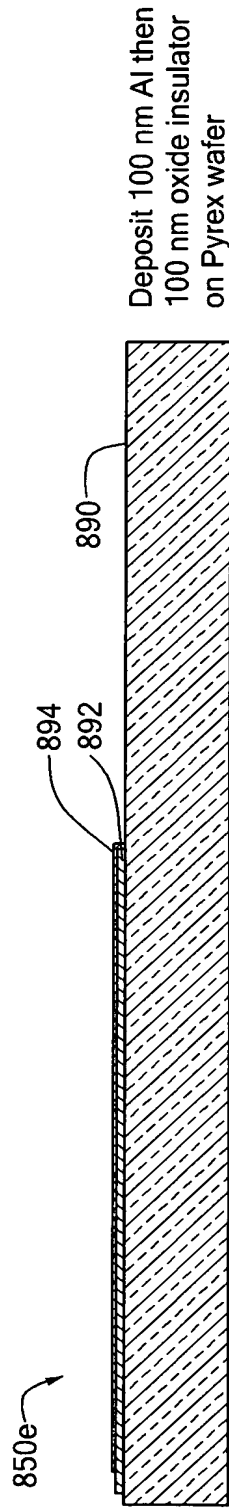


FIG. 16D

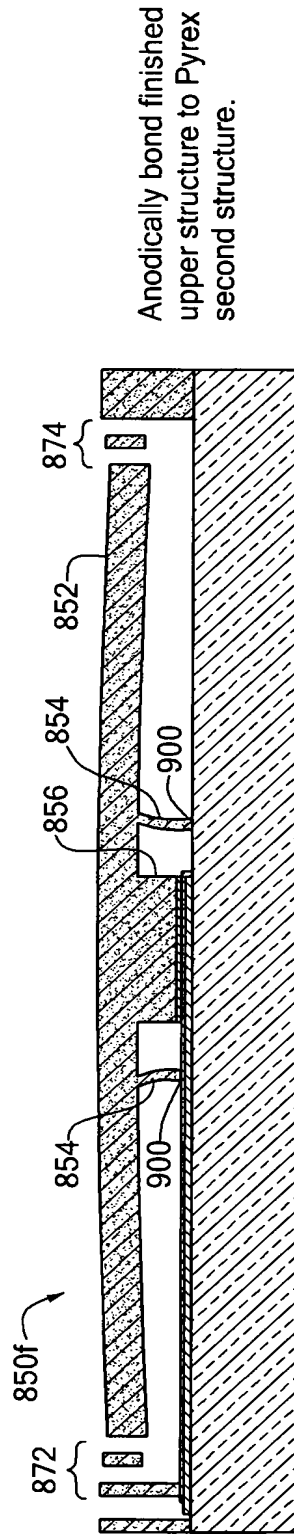
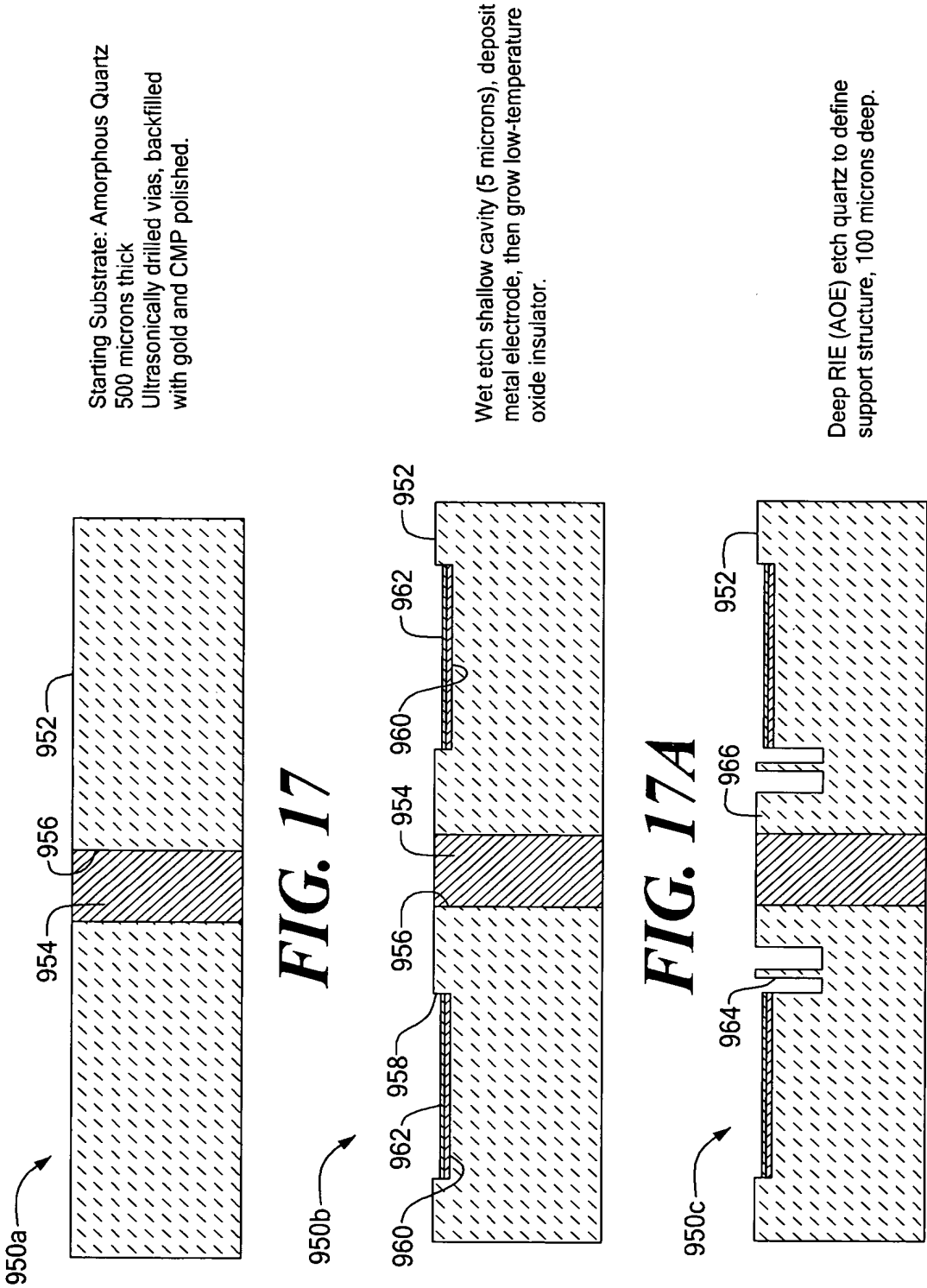
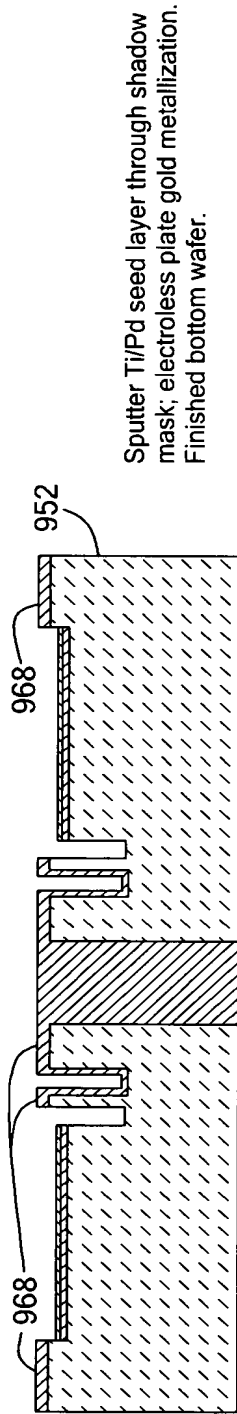


FIG. 16E

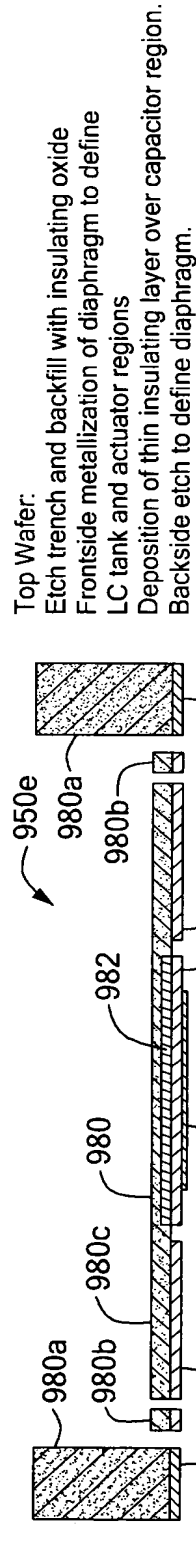






Sputter Ti/Pd seed layer through shadow mask; electroless plate gold metallization. Finished bottom wafer.

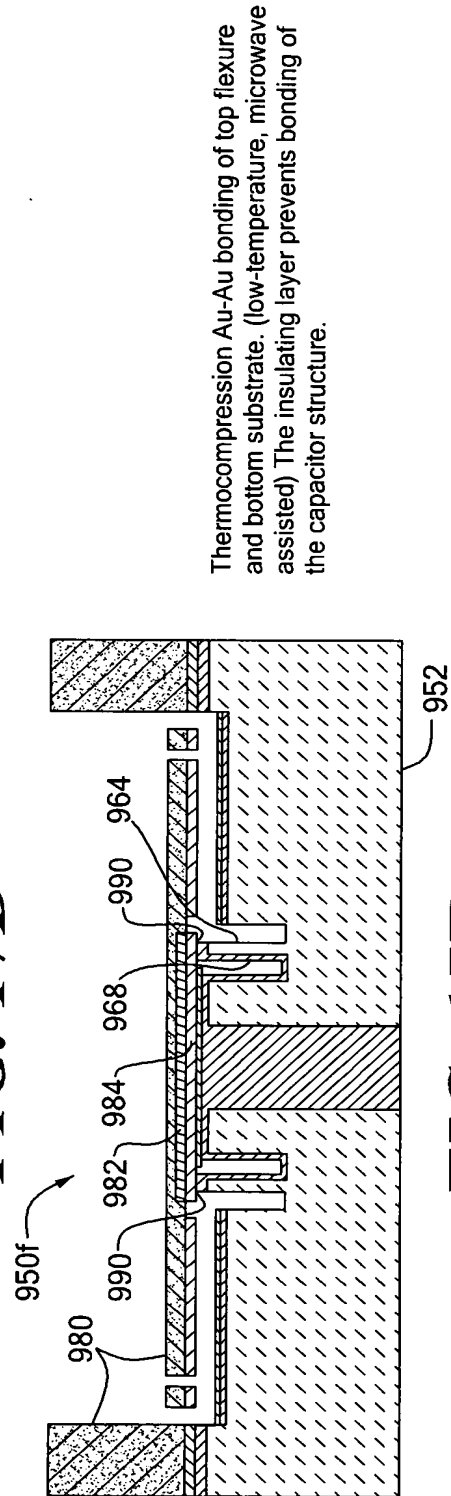
**FIG. 17C**



Top Wafer:

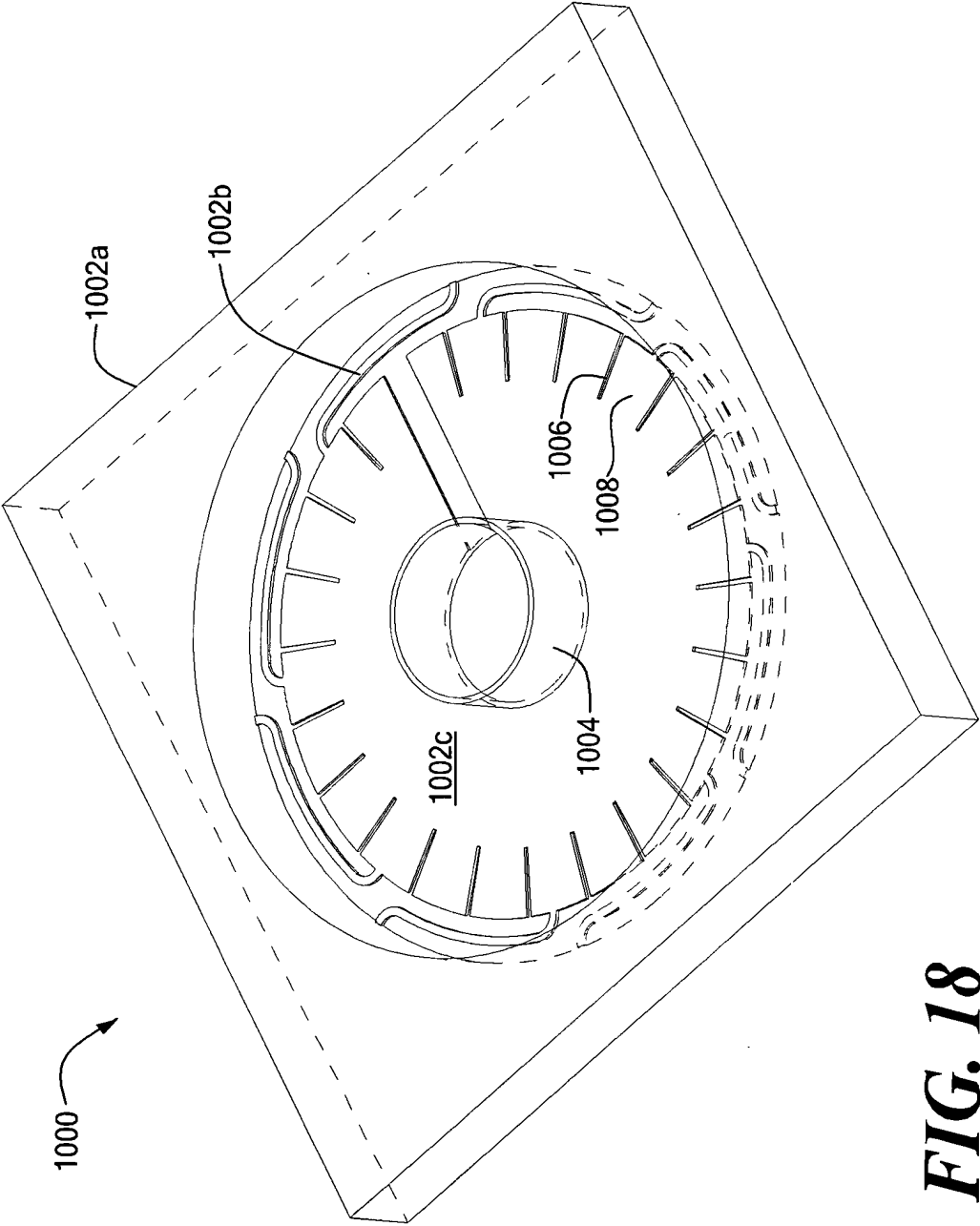
Etch trench and backfill with insulating oxide  
Frontside metallization of diaphragm to define LC tank and actuator regions  
Deposition of thin insulating layer over capacitor region.  
Backside etch to define diaphragm.

**FIG. 17D**

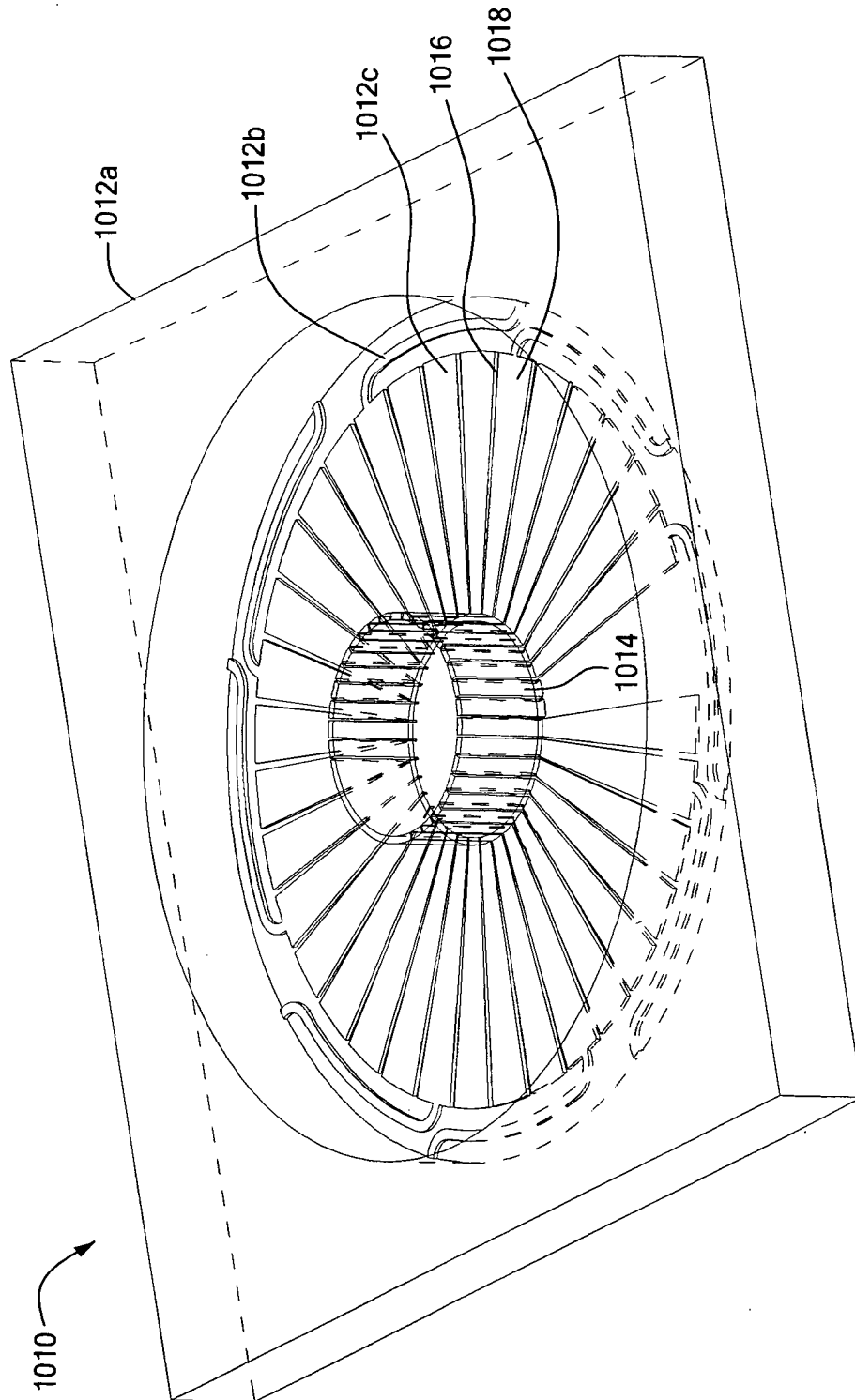


Thermocompression Au-Au bonding of top flexure and bottom substrate. (low-temperature, microwave assisted) The insulating layer prevents bonding of the capacitor structure.

**FIG. 17E**



**FIG. 18**



**FIG. 19**